Amendments to the Specification:

Please amend the specification as follows:

Amend the specification at the paragraph at page 2, lines 4 - 7, as follows:

The present application and application no. ~~--/---,---~~ 10/625,944 entitled "Receivers For Cycle Encoded Signals" (Docket No. 42P17324) were filed on ~~the same day~~ July 23, 2003, have identical specifications (except for titles, technical field description, claims, and abstract), and claim related subject matter.

Amend the specification at the paragraph at page 16, lines 12-16, as follows:

At time t3, the 1 T delay signal is rising, and Q1 and Q2 are 0 so that SR and SF both rise. Accordingly, flip-flop 336 clocks the 1 output by XOR 332 to Q1 and flip-flop 338 does not clock. Hence, Q1 changes to 1 and Q2 ~~remain~~ remains 0. With SR being 1, the output control signal from OR gate 344 is 1. With SF 1, the output of AND gate 342 is 1. With the output control signal being 1, MUXs 352 and 354 pass Q1 and Q1*, respectively.

Amend the specification at the paragraph at page 16, lines 17-25, as follows:

At time t3.5, the 1 T delay signal is falling and Q2 is 0 so SR falls. However, Q1 is 1 which forces SF to remain 1 even though the 1 T delay signal is falling. According, neither flip-flop 336 or 338 clocks data and Q1 remains 1 and Q2 remains 0. As such, receiver 316 keeps the output control signal or data from changing during mid-segment transitions by blocking OR gate 330 from changing SF when Q1 is 1 and the 1 T delay signal falls (as in the case of t3.5 and t4.5) or by blocking NOR gate 326 from changing SR when Q2 is 1 and the 1 T delay signal rises (as in the case of t6.5). With [[SR]] SF being 1, the output control signal stays 1 and MUXs 352 and 354 continue to pass Q1 and Q1*, respectively. The output of AND gate 342 stays high.

Amend the specification at the paragraph at page 16, line 26 - page 17, line 3 as follows:

At time t4, the 1 T delay signal is rising and Q2 is 0 so SR rises and flip-flop 336 clocks the 1 output by XOR 332 to Q1. Q1 is 1 which forces SF to remain 1. However, with 1 T delay rising, SF would be a 1 even if Q1 were 0. ~~Output and Q1 and Q2 are 0 so that SR and SF both rise.~~

~~Accordingly, flip-flop 336 passes the 1 output of XOR 332 to Q1 and flip-flop 338 does not clock. Hence, Q1 and Q2 remain 0.~~ Since SF remains 1, flip-flop 338 does not clock. With SR being 1, the output control signal stays 1 and MUXs 352 and 354 continue to pass Q1 and Q1*, respectively. The output of AND gate 342 stays high.

Amend the specification at the paragraph at page 17, lines 16-20, as follows:

At time t6.5, the 1 T delay signal is rising and Q2 is 1 so that SR stays 0. As mentioned, this blocks flip-flop 336 from clocking. Since Q1 is 0 and the 1 T delay signal is [[0]] 1, SF changes to 1 and flip-flop 338 does not clock. Therefore, Q1 and Q2 remain 0 and 1, respectively. Since the output control signal was 0 and SR is 0, the output control signal remains 0 even though SF is 1. Accordingly, MUXs 352 and 354 continue to pass Q2 and Q2*, respectively.

Amend the specification at the paragraph at page 17, lines 21-25, as follows:

At time t7, the 1 T delay signal is falling and Q1 is 0 so SF is falling. SR is also ~~falls~~ 0. Accordingly, flip-flop 338 clocks the 0 output by XOR 332 to Q2 and flip-flop 336 does not clock. Hence, Q2 changes to 0 and Q1 remains 0. With SF being 0, the output of AND gate 342 is 0. Further, since SR is 0, the output control signal is 0. With the output control signal being 0, MUXs 352 and 354 pass Q2 and Q2*, respectively.

Amend the specification at the paragraph at page 25, lines 2-9, as follows:

In some embodiments, the inventions includes a transmitter including a cycle encoding circuit to receive a data input signal and to provide a full cycle encoded signal in response thereto by continuously joining portions of different encoding signals. Some of the encoding signals have a different frequency than others of the encoding signals and some of the encoding signals have a different phase than others of the encoding signals. Data is represented in data time segments of the full cycle encoded signal and no data time segment has more than one cycle of an encoding signal. In some embodiments, a receiver receives the cycle encoded signal and recovers data of the data input signal. ~~Still other embodiments are described and claimed.~~